The interrupts are captured by PAL U29 and encoded into the signals IPL0, IPL1 and IPL2, which are input to the 68000. On receipt of a valid code, the 68000 begins an interrupt cycle. An interrupt acknowledge signal, IACK*, is then created by U28 and input to the 68000 on the VPA* pin to identify the interrupt type as "autovector". U29 stores all pending interrupts and presents them in priority order to the 68000. Once serviced, a captured interrupt must be cleared by the 68000 before lower priority interrupts can be input to it. This is done by writing to the "interrupt capture register" in U29.

3.1.3 Coprocessor Interface

The 68000 and the microcontroller communicate across a bi-directional 8-bit parallel interface which allows asynchronous, full-duplex data transfers. Identical interfaces are used to communicate with microcontrollers on the DPB and the optional ACON board.

The interface uses two octal latches for data transfer (U18, U20) and two flip-flops for handshaking (U9). U20 latches a byte of data for transfer from the 68000 to the microcontroller. U18 latches a byte for transfer in the other direction. The latches are accessed by the microcontroller on port 'C' (C0-C7), and by the 68000 on the LSB of its data bus (D0-D7). The microcontroller strobes WR-TO-68000 low when it writes data into U18. It strobes RD-68000 low when it reads data from U20. Either action generates an interrupt, IOP-I, which is detected by U29. In response, the 68000 software reads the 'interrupt status register' (U11) to determine if a read or write occurred. Handshaking signals IOP-WR and IOP-RD input to U11 indicate the state of the flip-flops (U9). IOP-WR and READY (the inverse of IOP-RD) are monitored by the microcontroller to detect access to the latches by the 68000.

On power-up of the projector, and whenever a software reset instruction is processed by the 68000, the flip-flops are cleared by the RESET* signal. As a result, the latches appear "empty" to both processors.

3.2 Waveform Generator

The primary function of the Waveform Generator is to produce convergence correction waveforms which are amplified by the Convergence Amplifier (CVA) and applied to the convergence coils of the red, green and blue CRTs. These waveforms also allow correction of raster geometry, both "global" (top pincushion, bottom pincushion and bow) and "zonal" (green convergence). The Waveform Generator also produces three horizontal rate dynamic focus waveforms for the Focus Module (FCM), one for each CRT.

Six control signals generated by the DPB are input to the Waveform Generator; WAVE-CLKB, CLK128B, START-CB, START-FB, V-DRIVE and HI-FREQ. WAVE-CLKB is a clock signal used for the convergence waveforms. It has approximately 256 cycles in the active horizontal scan when the horizontal frequency is below 80 kHz, and only 128 cycles at or above 80 kHz. CLK128B is a clock signal with approximately 128 cycles in the active scan. START-CB is a pulse occurring once every scan line which determines when the convergence waveforms begin. It anticipates the start of scan by several hundred nanoseconds to compensate for delay in the convergence coils. START-FB is a similar pulse which determines the start of the focus waveforms. It also anticipates the start of scan to compensate for delay in the focus coils. V-DRIVE is the vertical drive pulse. It resets the Waveform Generator's counter circuitry at the end of each video field. Finally, HI-FREQ is a control signal that goes low when the scan frequency is at or above 80 KHz.